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10/072,843	02/06/2002	Sehat Sutardja	MP0094	3730

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10-072,843	Applicant(s) Sehat
	Examiner SHINGLETON	Group Art Unit 2817

—Th MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 6-26-2003.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-21 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-6, 9-18, 20 and 21 is/are rejected.

☒ Claim(s) 7, 8, 19 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ Th specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Atta hment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 7

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Revi w, PTO-948

☐ Other _____

Office Acti n Summary

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 9-12, 14-16, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuyama et al. JP406061752A (Matsuyama) in view of Holt "Electronic Circuits digital and analog", pages 423, 431, 436 (Holt).

Figure 1 of Matsuyama discloses a nested transimpedance amplifier circuit having a "zero-order TIA", elements 2_1, 2_2 and 4, a first amplifier 2_3 having an input that communicates with the output of the zero-order TIA and an output, and a first feedback resistance in the form of a fixed resistor 3 has one end that communicates with the input of the zero-order TIA and an opposite end that communicates with the output of the first amplifier as is clearly shown in Figure 1 of Matsuyama. The abstract of Matsuyama sets forth "securing" a wide dynamic range i.e. the bandwidth is increased (see page 8, first full paragraph of the instant application.). Element 1 of Matsuyama is an optical sensor and thus the nested TIA of Matsuyama is clearly "implemented in an optical sensor". The abstract of Matsuyama also calls amplifiers 2_1, 2_2 and 2_3 inverting amplifiers. Matsuyama is silent on calling these amplifiers operational amplifiers (opamp) and only shows them as generic conventional structures. Matsuyama being silent on the specific structure of the amplifiers is likewise silent on whether these amplifiers include bipolar junction transistors. Claims like claim 11 recite the use of metal-oxide-semiconductor (MOSFET) transistors and the bandwidth having a value "greater than 10% of a threshold frequency"." Matsuyama does not show the TIA arrangement as being "implemented in a preamplifier of a hard disk drive." Matsuyama is also silent on the differential or balanced signal version of the amplifier. Matsuyama only shows the single ended version. Claims 14+ are directed toward the balanced signal version.

Holt discloses that the typical inverting amplifier circuit includes an opamp (See Figure 14.1 of Holt.). This is a conventional circuit. Holt also discloses that the conventional opamp can be composed of bipolar junction transistors (See page 431).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used operational amplifiers that employ bipolar junction transistors for the amplifiers 2_1, 2_2 and 2_3 because as the Matsuyama reference is silent on the exact amplifier circuit, any art-recognized equivalent amplifier circuit would have been useable therewith such as the conventional operational amplifier as shown in Holt.

The MOSFET is a common art recognized equivalent to that of the bipolar junction transistor.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ MOSFET transistors in place of the bipolar junction transistors for the amplifiers 2_1, 2_2 and 2_3 in the combination of Matsuyama and Holt as noted above because the MOSFET is a well known art-recognized equivalent transistor to that of the bipolar junction transistor. With the replacement of the bipolar with the MOSFET the bandwidth being greater than 10% of the threshold frequency is an obvious consequence of this combination.

It is well known engineering practice to form a balanced amplifier arrangement from that taught by a single amplifier arrangement. The differential amplifier is composed of two single ended amplifiers placed together in a mirror arrangement so as to be able to amplify a balanced or two-ended signal (See page 423 of Holt). Thus it would have obvious to one of ordinary skill in the art at the time the invention was made to "mirror" the arrangement of Matsuyama and Holt, i.e. provide two inputs/outputs and associated feedback loops for both "sides" of the amplifier so as to allow for the use of a balanced signal as taught by Holt.

Claims 2-6. 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuyama et al. JP406061752A (Matsuyama) in view of Holt "Electronic Circuits digital and analog", pages 423, 431, 436 as applied to claims 1, 9-12, 14-16, 20 and 21 above, and further in view of Bayruns et al. 5,646,573 (Bayruns) of record.

Matsuyama and Holt are both silent on the use of a capacitor having one end that communicates with the input of the zero-order TIA. Note that the obvious combination above results in two operational amplifiers in the zero-order TIA part of the combination. This meets the second and third opamp limitations of claim 3. With respect to claim 4 the second feedback resistance is recited as being on the third opamp which would be equivalent to amplifier 2_2 and the resistance 4 of Matsuyama. Claims 17 and 18 recite the equivalent in a "mirrored" arrangement that is merely the balanced signal version of the single ended version. The zero-order arrangement of Matsuyama is a series arrangement and it is common knowledge that one can rearrange the order of the series arrangement without changing the function of the series arrangement. This is just a mere rearrangement of the parts. Thus it would have

been obvious to on of ordinary skill in the art to rearrange the amplifiers 2_1 and 2_2 and their associated feedback loops for both the single ended version and the double ended versions as this results in the same function as is common knowledge in the art. Matsuyama and Holt also are silent on the addition of amplifiers both before and after the three-amplifier arrangement of Matsuyama and Holt (See claims 5 and 6). It is commonplace to cascade amplifiers in which the arrangement of Matsuyama and Holt is directed. The number of amplifiers is dependent on the desired gain one wants to achieve which is merely the selection of the optimum or workable range. A single amplifier may not provide the desired gain and thus multiple amplifiers would be needed to provide that gain. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide amplifiers in cascade before and after the cascade arrangement of Matsuyama so as to produce a desired gain which is within the optimum or workable range as is common knowledge in the art.

Bayruns discloses that it is commonplace to employ a capacitor C_1 coupled to the input of an amplifier so as to capacitively couple the output of the photo-detector to the input of the amplifier (See column 3, around line 50). This, as is common knowledge, blocks the DC that may be present on the input from being amplified by the amplifier so that one amplifies the desired time varying signal and not the static signal.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a capacitor having one end in communication with the zero-order TIA so as to block the DC signal and pass the desired time varying signal to the amplifier as taught by Bayruns.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuyama et al. JP406061752A (Matsuyama) in view of Holt "Electronic Circuits digital and analog", pages 423, 431, 436 as applied to claims 1, 9-12, 14-16, 20 and 21 above, and further in view of Jeppson 6,122,131 (Jeppson).

The reasoning as applied above is relates to the rejection of Matsuyama et al. JP406061752A (Matsuyama) in view of Holt "Electronic Circuits digital and analog", pages 423, 431, 436 as applied to claims 1, 9-12, 14-16, 20 and 21above and the following: Matsuyama et al. and Holt are silent on implementing the amplifier made obvious above in a preamplifier arrangement for a hard disk drive.

One common use for conventional amplifiers is that of a preamplifier for a hard disk drive as disclosed by Jepson (Note Figure 7). It is likewise conventionally known in the art that such amplifiers are to have high bandwidth so that high speed can be obtained.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the high bandwidth amplifier made obvious above as the preamplifier for a hard disk drive as Jeppson teaches any conventional preamplifier having high speed can be employed for the preamplifier of a hard disk drive.

Allowable Subject Matter

Claims 7, 8 and 19 are still objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's arguments filed 6-26-2003 have been fully considered but they are not persuasive. Applicant argues that the whole arrangement of Matsuyama et al. JP406061752A is part of a zero order TIA. Applicant does not dispute that that elements 2_1, 2_2 and 4 forms a zero order TIA. Applicant believes that claim 1 is directed to "something different" and goes on to recite a zero order TIA inserted or nested within additional components. The examiner respectfully disagrees, for what the examiner has identified as the zero order TIA is inserted or nested within additional components as recited by the claims and explained in the previous and present rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
Sept 20, 2003

MICHAEL B. SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817